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PATENT, TRADEMARK
AND COPYRIGHT LAW

FACSIMILE: (703) 684-1157

Date: August 15, 2000

Attorney Docket No. NIT-217

To: Assistant Commissioner for Patents
Washington, D.C. 20231

Sir: Transmitted herewith for filing is the patent application of:

Inventor: T. OHKAWA et al (See Attached List)

For:
RFID (RADIO FREQUENCY IDENTIFICATION) AND IC CARD

Enclosed are:

- [X] 6 Sheets of Drawings
- [ ] This application is being filed without an executed Declaration.
- [X] Priority is claimed from Japanese Application No. 2000-067141 filed March 7, 2000. [ ] A certified copy is attached herewith.
- [X] Copies of the disclosure documents listed on the attached PTO 1449 form and [X] discussed in the specification or [ ] attached Information Disclosure Statement.
- [ ] A verified statement to establish small entity status under 37 CFR 1.9 and 1.27.
- [X] Specification: Abstract X, Description 15 pages; and 10 claim(s).
- [ ] Preliminary Amendment.
- [X] Executed Declaration.

The filing fee is calculated as shown below:

For:	No. Filed	No. Extra	Small Entity Rate	Small Entity Fee	OR	Large Entity Rate	Large Entity Fee
Basic Fee				$ 345			$ 690
Total Claims	10 -20 =	* 0	x 9	$		x 18	$ 0
Indep Claims	8 - 3 =	* 5	x 39	$		x 78	$ 390
[ ] Multiple Dependent Claim (s)			+ 130	$		+ 260	$ 0
			Total	$		Total	$ 1,080

* If difference is less than zero then enter '0' in second column

- [X] A check in the amount of $ 1,080.00 is enclosed for the filing fee.
- [X] The Commissioner is hereby authorized to charge any additional fees that may be required to Deposit Account No. 50-1417.

Respectfully Submitted,

By: [signature]
John R. Mattingly
Registration No. 30,293

NIT-217
NT0144US

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Title of the Invention

RFID (RADIO FREQUENCY IDENTIFICATION) AND IC CARD

Inventors

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RFID (RADIO FREQUENCY IDENTIFICATION) AND IC CARD

BACKGROUND OF THE INVENTION

The present invention relates to a radio frequency identification (RFID) and an IC card for the RFID, and more particularly to an RFID and a contactless IC card containing the same for receiving power and information from an external apparatus and for transmitting information to the external apparatus on a contactless basis.

An RFID is used as a tag, for example, and an IC card is a kind of the RFID.

In a conventional RFID such as contactless IC card and the like in which power is received from an external apparatus and signals are interchanged with the external apparatus on a contactless basis, an AC wave received by an antenna coil is rectified and smoothed and then supplied to internal circuits through a series regulator. Recently, however, for the purpose of widening a working voltage margin, there has also been used a method of supplying power only by providing a limiter circuit for high voltage resistant protection after rectification and smoothing, without using a series regulator in which a voltage loss is inevitable.

As a power-on-reset circuit for maximizing a working voltage margin, it is common practice to use a hysteresis circuit having a two-stage structure wherein, for countermeasure to

dynamic load variation by internal circuits, a reset voltage is given at a level of a logic working guarantee voltage in a steady state and the sum of the logic working guarantee voltage and a voltage for compensating for a voltage drop due to dynamic load variation is used as a power-on-reset release voltage. This circuit scheme is disclosed in Japanese Patent Laid-open (Kokai) No. Hei 10-207580, for example. Further, in Japanese Patent Laid-open (Kokai) No. Hei 8-30752, there is disclosed a circuit arrangement of a contactless IC card using a series regulator wherein, for compensating for a voltage drop in operation of a CPU contained in the IC card, a dummy load corresponding to a CPU operation load is applied before release of power-on-resetting and the dummy load is removed at the time of release of power-on-resetting.

SUMMARY OF THE INVENTION

The above-mentioned circuit arrangement disclosed in Japanese Patent Laid-open (Kokai) No. Hei 8-30752 is disadvantageous in that there is difficulty in application to RFID in which dynamic impedance variation by such means as intermittent load operation is used for communication from an IC card to an external apparatus (this kind of technique is defined in ISO 10536 and ISO 14443). Although it is possible to apply this circuit arrangement to RFID by superimposing a communication load on the dummy load, there arises a problem

that the dummy load must be redesigned according to design changes in load for communication and design changes in antenna coil. Further, the dummy load must be set to have a value inclusive of upper limits of individual CPU difference, individual communication load difference, and impedance variation with temperature, resulting in a problem that a startup receiving power level higher than an operational receiving power level is required. Moreover, the complexity of this circuit arrangement gives rise to a problem of an increase in cost.

As noted above, for communication to an external apparatus defined in ISO 10536 and ISO 14443, there is a technique of dynamic impedance variation by such means as intermittent load operation. In implementation of RFID using this technique, a reset release voltage used in a hysteresis power-on-reset circuit such as disclosed in Japanese Patent Laid-open (Kokai) No. Hei 10-207580 must be set to have a value corresponding to the sum of a working guarantee voltage and a drop-down voltage inclusive of an upper limit of individual communication load difference (inclusive of impedance variation with temperature), resulting in a problem that a margin of a startup voltage is narrowed. Further, with a design change in load for communication or a change in impedance related with a transmission system connected from an IC card to an external apparatus, e.g., with a design change in antenna coil, it is

inevitable to redesign a power-on-reset release voltage. Still further, there arises a problem of an increase in circuit complexity.

In a contactless IC card defined in ISO 10536 and ISO 14443, an AC wave received by an antenna coil is rectified and smoothed to provide power source to internal elements of an IC, and communication with an external apparatus is carried out by varying a load on the IC. Thus, a variation width of a power supply voltage of the IC is rather large. Therefore, the power supply voltage is monitored at all times to check whether or not it is within a working guarantee range of the IC. If the power supply voltage is within the working guarantee range, a reset state imposed on the IC is released to operate internal circuits thereof. In this scheme, a hysteresis circuit configuration of a two-stage type is provided in which a reset voltage is given at a working guarantee voltage level and the sum of the reset voltage and a voltage drop due to dynamic load variation is used as a reset release voltage. This condition is a cause of reducing a working voltage margin of the IC.

As described above, in conventional contactless IC cards and RFIDs, the settings of a dummy load and a reset release voltage involve external factors, causing a disadvantage of the lack of general versatility and a difficulty in ensuring a maximum of a working voltage range.

It is therefore an object of the present invention to

obviate the above-mentioned disadvantages by providing an RFID, using dynamic impedance variation by such means as intermittent load operation for communication to an external apparatus defined in ISO 10536 and ISO 14443, wherein, when a data communication circuit of the IC is in a reset state, the IC is put in a low impedance state for communication, and wherein, when a coupling force between the external apparatus and the RFID is equivalent to or higher than that at release of resetting, a reset action is not performed at the time of voltage drop due to impedance variation as a method of communication after release of resetting.

Although the present invention will be described in detail as related to an IC card, it is to be understood that the present invention is applicable to other implementation forms of RFID. In the following detailed description of the preferred embodiments, an IC card containing a microprocessor will be taken as an example. In addition, an IC card comprising logic elements without using a microprocessor is also within the scope of the present invention. Furthermore, while a contactless IC card having an antenna will be discussed in the following detailed description, the present invention is applicable to a contact-type IC card and a contactless IC card having no antenna.

The above and other objects, features and advantages of the present invention will become more apparent from the

following detailed description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic illustration showing a part mounting arrangement on an IC card;

FIG. 2 is an IC card circuit block diagram;

FIG. 3 is a diagram showing a reference example of a modulator part in an IC;

FIG. 4 is an operation timing chart of each part in the circuit structure shown in FIG. 3;

FIG. 5 is a diagram for detailed description of DC power voltage variation in connection with the timing chart shown in FIG. 4;

FIG. 6 is a diagram showing a modulator part in an IC in a preferred embodiment of the present invention;

FIG. 7 is a diagram for detailed description of DC power voltage variation in connection with the timing chart shown in FIG. 6;

FIG. 8 is a diagram for detailed description of DC power voltage variation in connection with the timing chart shown in FIG. 7; and

FIG. 9 is a diagram showing a modulator part in an IC in another preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail by way of example with reference to the accompanying drawings.

Embodiment 1:

A configuration and circuit operations of a contactless IC card as a form of RFID will first be described below.

FIG. 1 presents a general configuration of the contactless IC card. In this figure, there is shown a plan view of a part mounting arrangement on a card base material with a surface layer removed. An IC chip 2 is connected with an antenna coil 3 on an IC card 1.

FIG. 2 presents a general configuration of circuit blocks of the contactless IC card. The circuit block configuration shown in this figure is applicable to implementation of the present invention. Note, however, that an internal structure of a power-on-reset circuit 7 in the present invention is different from those in conventional techniques.

Referring to FIG. 2, power is received from an external apparatus through the antenna coil 3 contained in the IC card 1. For information interchange with the external apparatus, contactless coupling operations are performed as described below.

An AC wave having a predetermined frequency, received by the antenna coil 3 from the external apparatus, is converted into DC power through a rectifying-smoothing circuit 4 in the

IC chip 2. Then, at a DC voltage level corresponding to an upper limit imposed by a limiter circuit 5 for overvoltage protection, the DC power is supplied to each internal circuits. Meanwhile, with the AC wave received by the antenna coil 3, it is detected that the DC voltage is higher than a voltage level predetermined for the power-on-reset circuit 7. Under this condition, each circuit in a data communication circuit 6 is released from a reset state to enter an active state. The AC wave received by the antenna coil 3 is fed to a demodulator-clock generator circuit 61, which then generates a clock signal to a processor 8. Using the clock signal thus generated, a reset circuit 63 produces a reset signal for activating the processor 8 with predetermined timing. Thus, the processor 8 is supplied with the reset signal. Information from the external apparatus is received by the IC card 1 through phase modulation of an AC wave. Then, the phase-modulated AC wave is demodulated by the demodulator - clock generator circuit 61, and demodulated information is supplied to the processor 8. A carrier signal used for information transmission from the IC card 1 to the external apparatus is generated by a carrier signal generator circuit 62 which divides a frequency of the clock signal to a predetermined frequency. The carrier signal is phase-modulated with data signal from the processor 8 by a modulator 64. FETs 9 and 10 are switched by an output of the modulator 64 to intermittently turn on-off resistors 11 and 12 disposed

between terminals of the antenna coil 3 and circuit ground, thereby producing impedance variation in the IC chip 2. That is to say, through the use of the carrier signal phase-modulated with the data signal, dynamic impedance variation is produced in the IC card 1. Detecting the dynamic impedance variation by the carrier signal in the IC card 1, the external apparatus performs phase demodulation to attain information signals from the IC card 1.

Then, using FIGS. 3, 4 and 5, the following describes operations of a reference example of a modulator 64 and peripheral circuits thereof.

FIG. 3 shows a detailed structure of the modulator 64 and an impedance control circuit in a reference example. In this example, it is inevitable to employ a power-on-reset circuit having a hysteresis characteristic.

When a DC power supply voltage reaches a predetermined reset release voltage level, a power-on-reset signal from the power-on-reset circuit 7 connected with an R (reset input) terminal of a flip-flop 64a is made to have a low level, causing the flip-flop 64a to be put in an active state.

The carrier generator circuit 62 is also put in active state to generate a carrier signal. The carrier signal thus generated is applied to a CLK (clock input) terminal of the flip-flop 64a and an input terminal of an exclusive-OR circuit 64b. The other input terminal of the exclusive-OR circuit 64b

is connected with a Q (output) terminal of the flip-flop 64a, and an output terminal of the exclusive-OR circuit 64b is connected with gate terminals of the FETs 9 and 10 used as switching elements. At a point of time when an input to the CLK terminal is changed from a low level to a high level, the flop-flop 64a operates so that a level state of a data signal from the processor 8 connected with a D (data input) terminal is output through the Q terminal. Therefore, until a change occurs in the data signal, the Q terminal remains at a low level, and the carrier signal is fed in intact state to the output terminal of the exclusive-OR circuit 64b. In a state that the data signal has a high level, an inverted signal of the carrier signal is output through the output terminal of the exclusive-OR 64b. Consequently, according to a level of the data signal, the modulator 64 acts to perform phase inversion in synchronization with the carrier signal.

The FETs 9 and 10 used as switching elements turn on when a gate input level is high, and they turn off when the gate input level is low. Thus, when the FETs 9 and 10 turn on, the resistors 11 and 12 connected with the terminals of the antenna coil 3 are grounded to decrease impedance in the IC 2.

FIG. 4 presents an operation timing chart of each part described above in a situation where, after the start of high-frequency AC power supply from the external apparatus, the progress of DC power supply voltage is made up in a condition

high-frequency AC power supply voltage slightly exceeding a power-on-reset release voltage.

As can be seen from this timing chart, after release of resetting, a load for communication is intermittently applied to the antenna coil terminals in conventional arrangements. In the power-on-reset circuit, it is required as an indispensable condition to provide a hysteresis characteristic, i.e., a changeover function for selecting a reset release voltage level at the time of power-on or a reset voltage level for guaranteeing operations after release of resetting.

With reference to FIG. 5, the following describes details of operation behavior at the time of a rise of the DC power supply voltage indicated in FIG. 4.

As shown in FIG. 5, a reset release voltage in the power-on-reset circuit must be higher than the sum of a logic working guarantee voltage (a reset voltage after the start of circuit operation) and a drop-down voltage due to a load resistance for communication. The drop-down voltage is given to have a value inclusive of an error in fabrication process of communication load resistors and variation with temperature thereof. That is to say, an IC working range is narrowed due to the characteristic of the power-on-reset circuit as the indispensable condition regardless of effective operability.

Then, with reference to FIGS. 6, 7 and 8, the following describes operations of a modulator 64 and peripheral circuits

thereof in a preferred embodiment of the present invention.

FIG. 6 shows a detailed structure of the modulator 64 and an impedance control circuit according to the preferred embodiment of the present invention.

In this circuit arrangement, a power-on-reset circuit is so formed that a reset release voltage is equal to a reset voltage after the start of circuit operation, i.e., a simple circuit configuration can be provided.

When a DC power supply voltage reaches a predetermined reset release voltage level, a power-on-reset signal from the power-on-reset circuit 7 connected with an R (reset input) terminal of a flip-flop 64a is made to have a low level, causing the flip-flop 64a to be put in an active state.

The carrier generator circuit 62 is also put in an active state to generate a carrier signal. The carrier signal thus generated is applied to a CLK (clock input) terminal of the flip-flop 64a and an input terminal of an exclusive-OR circuit 64b. The other input terminal of the exclusive-OR circuit 64b is connected to a Q (output) terminal of the flip-flop 64a through an inverter 64c, and an output terminal of the exclusive-OR circuit 64b is connected with gate terminals of the FETs 9 and 10 used as switching elements. At a point of time when an input to the CLK terminal is changed from a low level to a high level, the flip-flop 64a operates so that a level state of a data signal from the processor 8 connected with a

D (data input) terminal is output through the Q terminal. Therefore, until a change occurs in the data signal, an output terminal of the inverter 64c remains at a high level, and the carrier signal is inverted and fed to the output terminal of the exclusive-OR circuit 64b. In a state that the data signal has a high level, the carrier signal is output as it is through the output terminal of the exclusive-OR circuit 64b. Consequently, according to a level of the data signal, the modulator 64 acts to perform phase inversion in synchronization with the carrier signal.

The FETs 9 and 10 used as switching elements turn on when a gate input level is high, and they turn off when the gate input level is low. Thus, when the FETs 9 and 10 turn on, the resistors 11 and 12 connected with the terminals of the antenna coil 3 are grounded to decrease impedance in the IC 2.

FIG. 7 presents an operation timing chart of each part described above.

As can be seen from this timing chart, the present invention provides a circuit arrangement in which a load for communication is applied to the antenna coil terminals at the time of resetting. In the power-on-reset circuit, it is therefore not required to provide a hysteresis characteristic.

FIG. 8 is a diagram for detailed description of operation behavior at the time of a rise of the DC power supply voltage in the timing chart shown in FIG. 7.

As shown in FIG. 8, a reset release voltage in the power-on-reset circuit is substantially equal to a logic working guarantee voltage (a reset voltage after the start of circuit operation). Therefore, no substantial adverse effect takes place due to an error in fabrication process of communication load resistors, variation with temperature thereof, design modification thereof, design modification of the antenna coil, and impedance variation in a transmission system including the external apparatus. Thus, it is possible to ensure a maximum of a working voltage range in the IC.

Embodiment 2:

Referring to FIG. 9, there is shown a partial circuit structure in an IC according to another preferred embodiment of the present invention.

In FIG. 9, the FETs 9 and 10 and the resistors 11 and 12 perform operations as described in the foregoing (explained in description in connection with FIGS. 3 and 7). An OR circuit 64d is provided between an output terminal of the modulator 64 in the data communication circuit 6 of the IC 2 as a switch operation signal source and the gate terminals of the FETs 9 and 10. As another input to the OR circuit 64d, a power-on-reset signal is applied from the power-on-reset circuit 7. There is provided a circuit arrangement in which an output of the OR circuit 64d has a high level when the power-on-reset signal is high regardless of an output level of the modulator 64. Thus,

at the time of resetting, the resistors 11 and 12 are grounded to decrease impedance in the IC 2. That is to say, it is not required to provide a hysteresis characteristic in the power-on-reset circuit. A maximum of a working voltage range in the IC can be ensured by establishing a reset level at a circuit working guarantee voltage.

According to the preferred embodiments of the present invention, it is not required to use a complex reset circuit in the IC. Further, only a logic working guarantee voltage is a required condition for establishing a reset voltage level, and there occurs no adverse effect due to impedance variation in the transmission system including the external apparatus. Therefore, an RFID having general versatility higher than conventional RFIDs can be realized at low cost.

The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The present embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the invention being indicated by the appended claims rather than by the foregoing description and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.

What Is Claimed Is:

1. An RFID comprising:

an antenna for receiving power to drive a semiconductor circuit device and for transmitting and receiving signals; and

first means for releasing a reset state of said semiconductor circuit device upon detection of a condition that a voltage attained by rectifying an AC wave induced on said antenna is higher than a predetermined voltage level;

wherein, when said reset state is released, information can be transmitted from said antenna to an external apparatus according to signals which are generated in said semiconductor circuit device by controlling a state of impedance of said semiconductor circuit device, and

wherein, in said reset state, said impedance is maintained at a low state.

2. An RFID according to claim 1,

wherein a reset release voltage used by said first means is substantially equal to a logic working guarantee voltage of an IC being a part of said RFID.

3. An RFID according to claim 2,

wherein, said reset release voltage is equal to a reset voltage applied after the start of logic working of the IC after releasing said reset state.

4. An RFID comprising:

an antenna; and

first means for releasing a reset state of a semiconductor circuit device upon detection of a condition that a DC voltage attained by rectifying an AC wave induced on said antenna is higher than a threshold level;

wherein, when said reset state is released, signal transmission from said antenna to an external apparatus can be performed according to signals which are generated in said semiconductor circuit device by controlling a state of impedance of said semiconductor circuit device,

wherein, when said DC voltage is lower than said threshold level, said semiconductor circuit device is put in said reset state, and

wherein, in said reset state, said impedance is decreased to a low state.

5. An RFID comprising:

an integrated circuit element having memory means, logic processing means, and power-on-reset means; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said memory means and logic processing means;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state.

6. An RFID comprising:

an integrated circuit element having communication means,

a logic circuit and power-on-reset means; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said IC device is maintained at a low state, and

wherein, when a reset state is released, signal transmission from said antenna to said external apparatus is performed according to signals which are generated in said integrated circuit element by controlling a state of said impedance of said integrated circuit element.

7. An RFID comprising:

an integrated circuit element having memory means, logic processing means and power-on-reset means;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state.

8. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means;

wherein, when a voltage applied to said power-on reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state, and

wherein, when a rest state is released, signal

transmission to an external apparatus is performed according to signals which are generated in said integrated circuit element by controlling a state of said impedance of said integrated circuit element.

9. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, impedance of said integrated circuit element is maintained at a low state, and

wherein, when a reset state is released, signal transmission from said antenna to said external apparatus is performed according to signals which are generated in said integrated circuit element by repeating an operation that a terminal of a load resistor whose another terminal is connected with a terminal of a coil of said antenna is connected to ground potential through a switching element and an operation that said terminal of said load resistor is disconnected from said ground potential by said switching element.

10. An RFID comprising:

an integrated circuit element having communication means, a logic circuit and power-on-reset means; and

an antenna for receiving power and signals from an external apparatus and for supplying said power and signals to said communication means and logic circuit;

wherein, when a voltage applied to said power-on-reset means is lower than a threshold level, a terminal of a load resistor whose another terminal is connected with a terminal of a coil of said antenna is connected to ground potential through a switching element.

ABSTRACT

An RFID which provides a wide working voltage range and general versatility at low cost, without the need for changing its internal circuit design due to external factors. In the RFID, there is provided an arrangement that a low impedance state is given when its internal data communication circuit is in a reset state.

FIG. 1

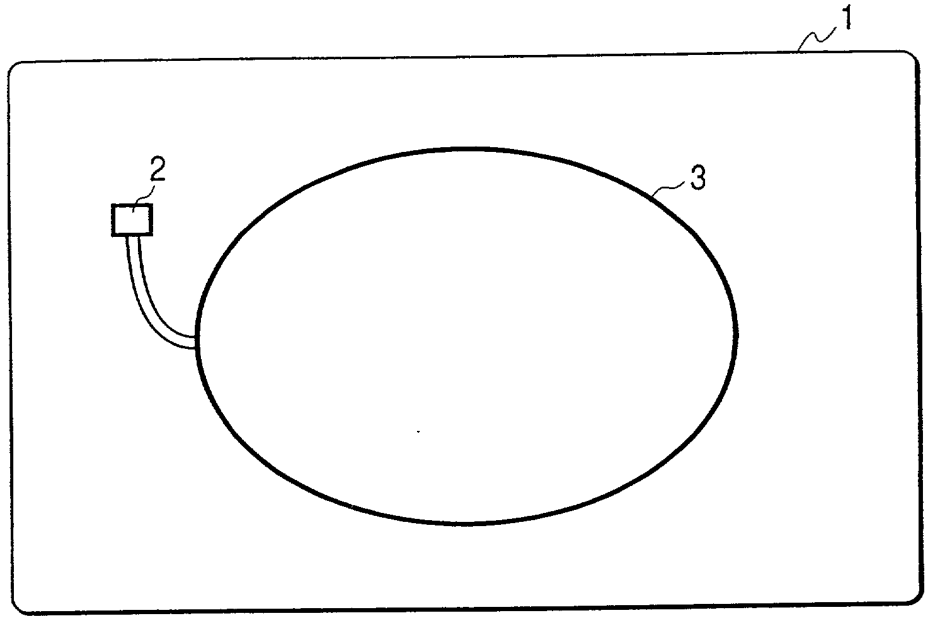

1
2
3

FIG. 3

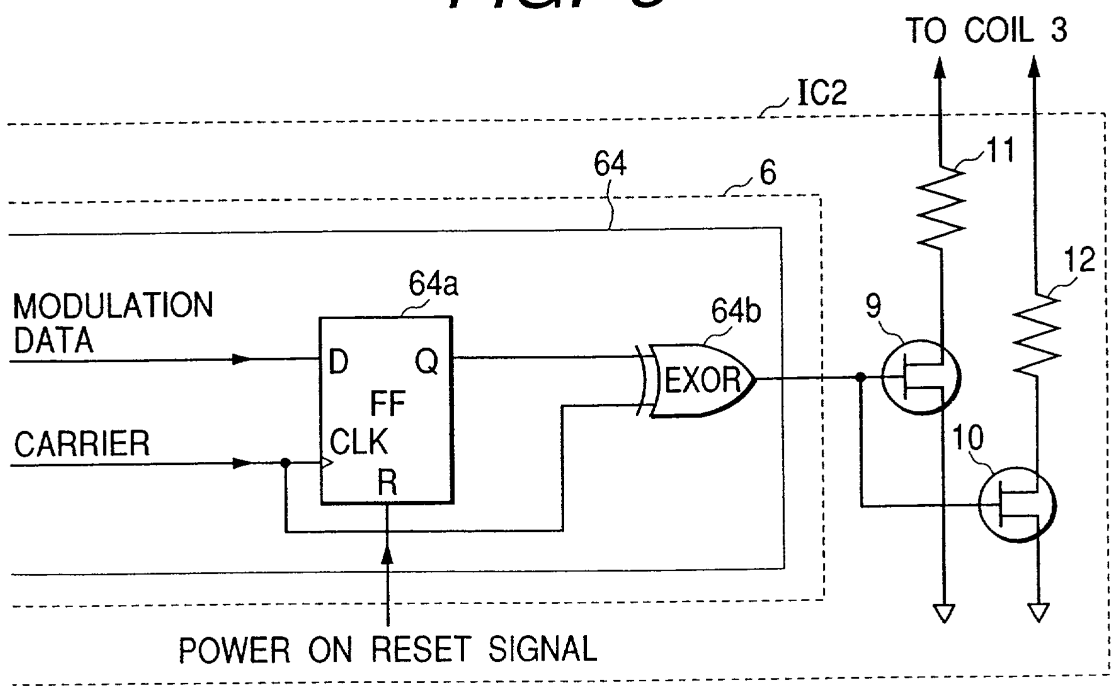

TO COIL 3
IC2
64
6
11
12
64a
64b
9
MODULATION DATA
D
Q
FF
EXOR
CARRIER
CLK
R
10
POWER ON RESET SIGNAL

FIG. 2

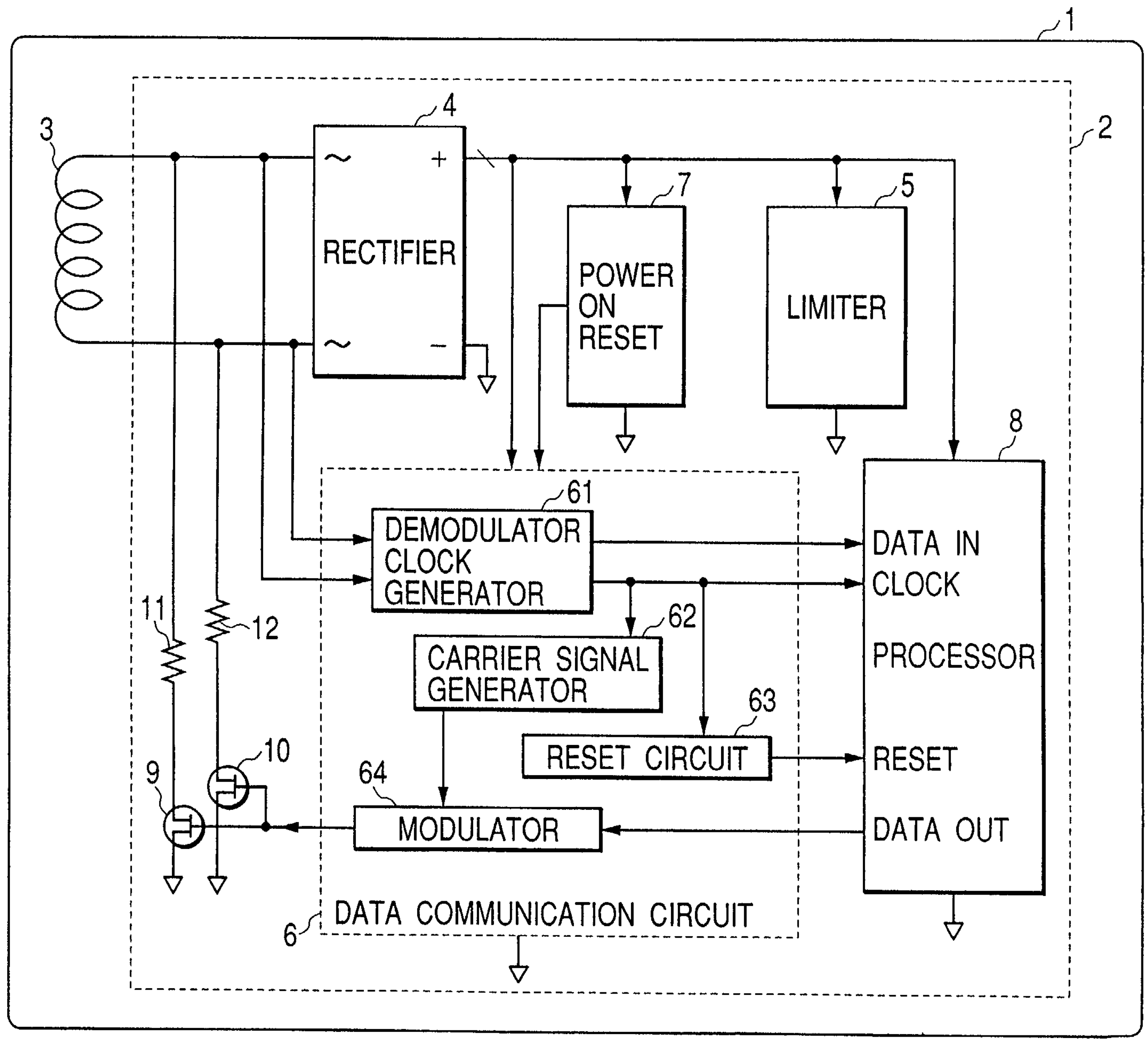

1
2
3
4
RECTIFIER
7
POWER
ON
RESET
5
LIMITER
8
61
DEMODULATOR
CLOCK
GENERATOR
62
CARRIER SIGNAL
GENERATOR
63
RESET CIRCUIT
64
MODULATOR
DATA IN
CLOCK
PROCESSOR
RESET
DATA OUT
6
DATA COMMUNICATION CIRCUIT
9
10
11
12

FIG. 4

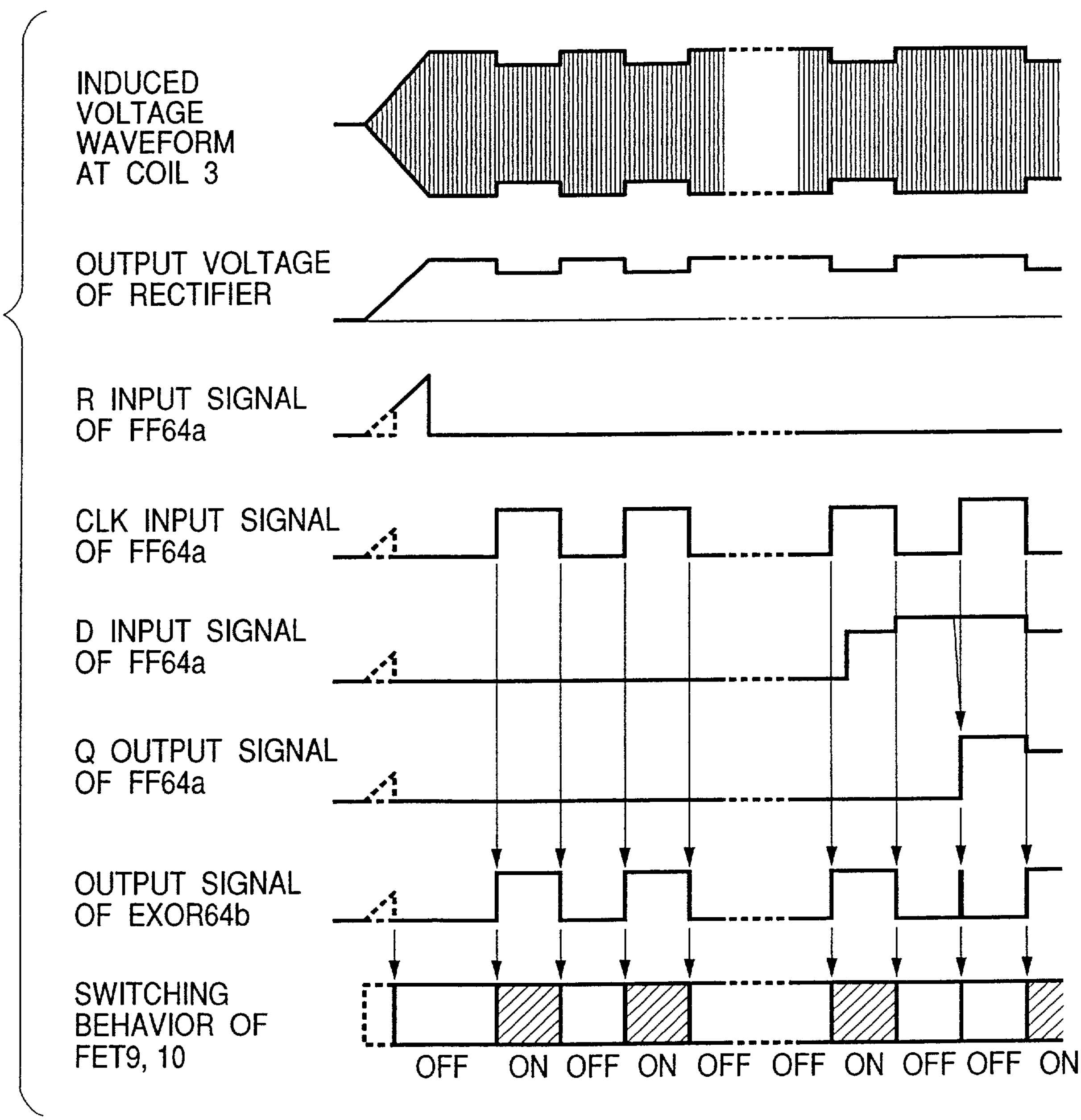

INDUCED VOLTAGE WAVEFORM AT COIL 3
OUTPUT VOLTAGE OF RECTIFIER
R INPUT SIGNAL OF FF64a
CLK INPUT SIGNAL OF FF64a
D INPUT SIGNAL OF FF64a
Q OUTPUT SIGNAL OF FF64a
OUTPUT SIGNAL OF EXOR64b
SWITCHING BEHAVIOR OF FET9, 10
OFF ON OFF ON OFF OFF ON OFF OFF ON

FIG. 5

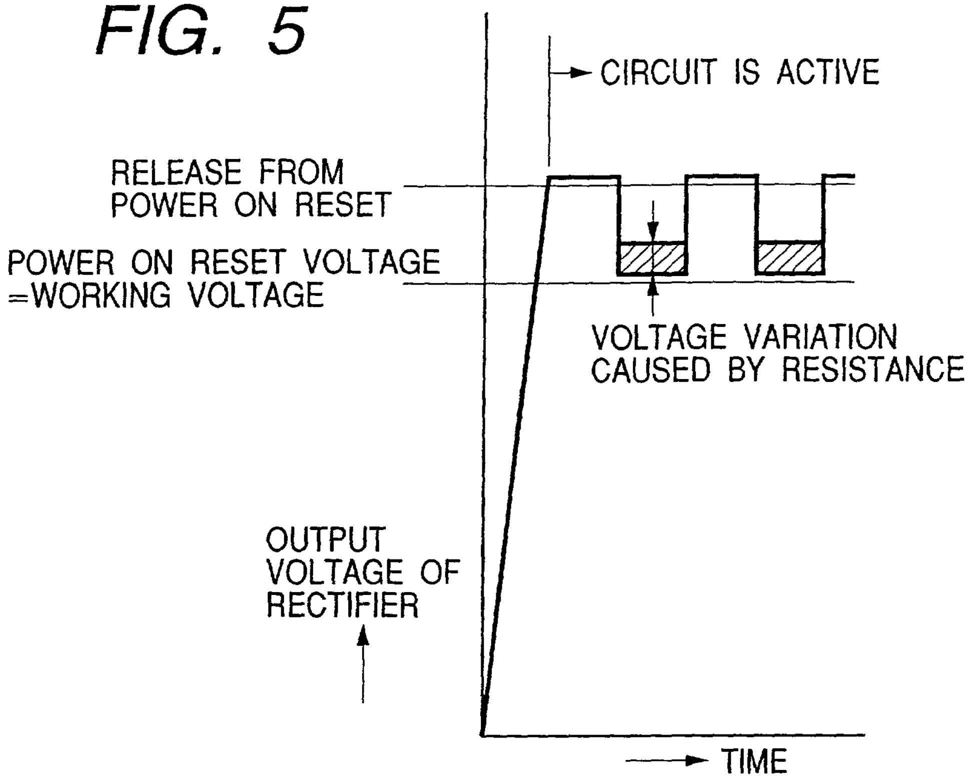

CIRCUIT IS ACTIVE
RELEASE FROM POWER ON RESET
POWER ON RESET VOLTAGE =WORKING VOLTAGE
VOLTAGE VARIATION CAUSED BY RESISTANCE
OUTPUT VOLTAGE OF RECTIFIER
TIME

FIG. 6

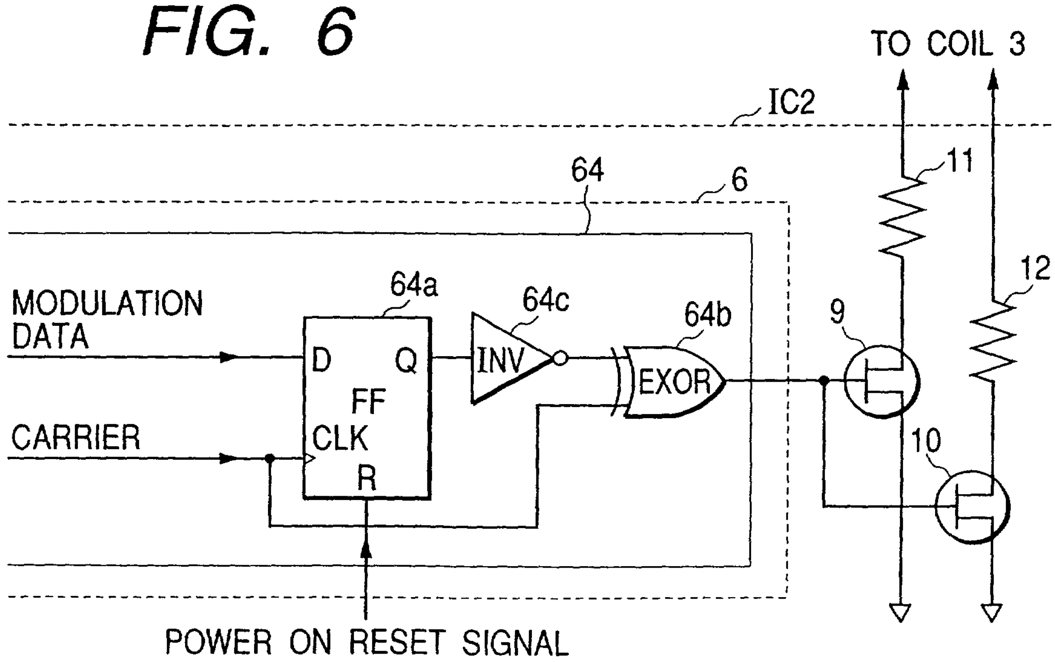

TO COIL 3
IC2
64
6
11
12
MODULATION DATA
64a
64c
64b
9
D
Q
FF
INV
EXOR
CARRIER
CLK
R
10
POWER ON RESET SIGNAL

FIG. 7

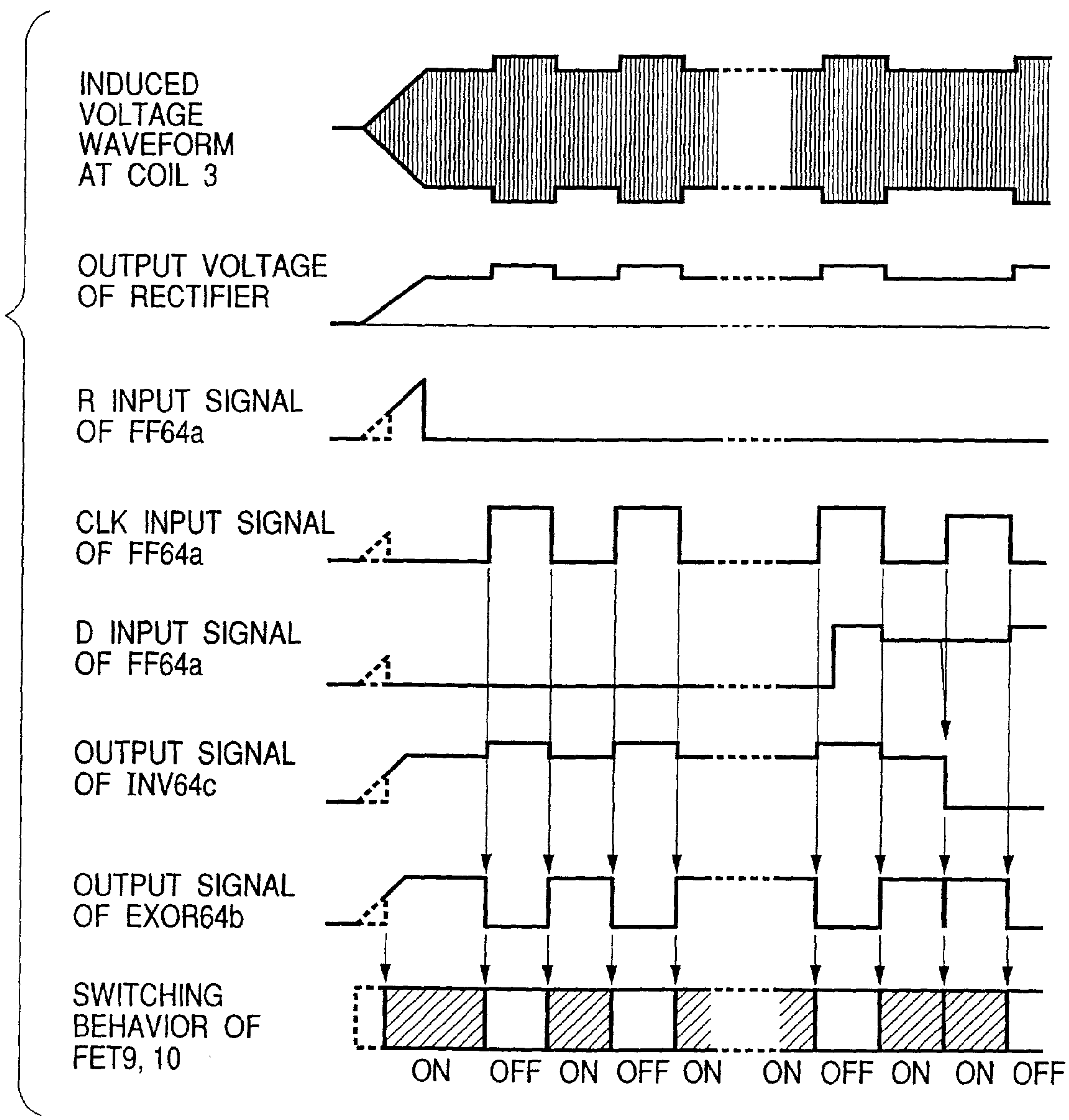

INDUCED VOLTAGE WAVEFORM AT COIL 3
OUTPUT VOLTAGE OF RECTIFIER
R INPUT SIGNAL OF FF64a
CLK INPUT SIGNAL OF FF64a
D INPUT SIGNAL OF FF64a
OUTPUT SIGNAL OF INV64c
OUTPUT SIGNAL OF EXOR64b
SWITCHING BEHAVIOR OF FET9, 10
ON OFF ON OFF ON ON OFF ON ON OFF

FIG. 8

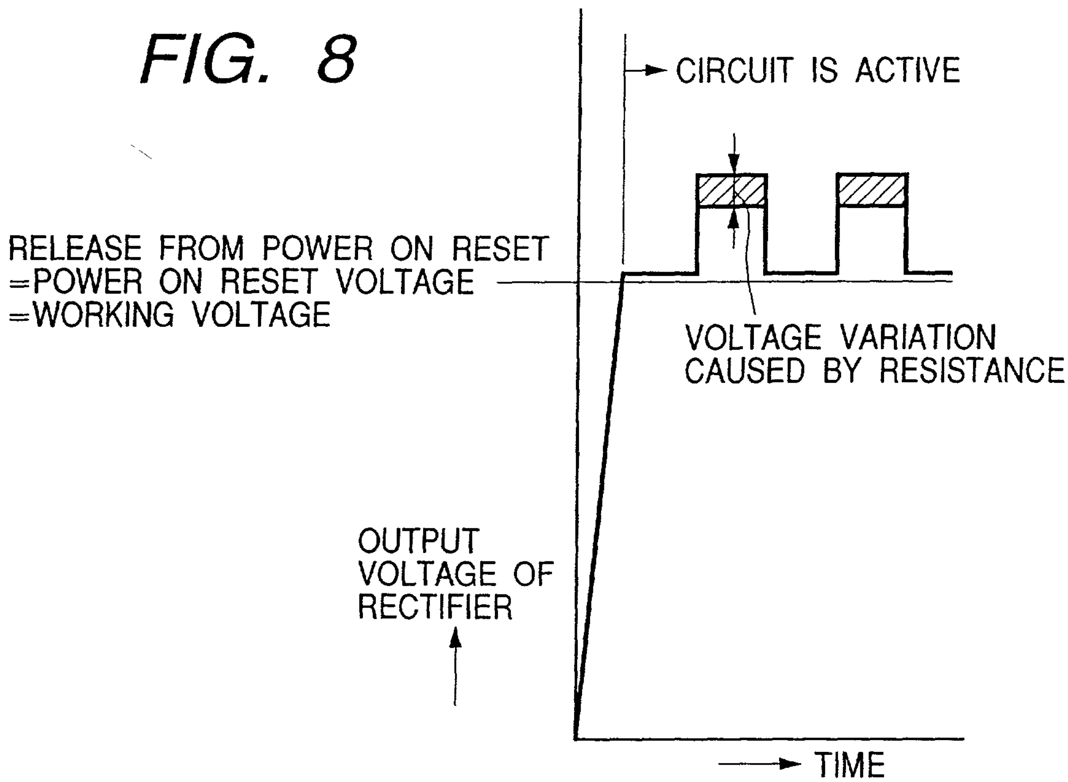
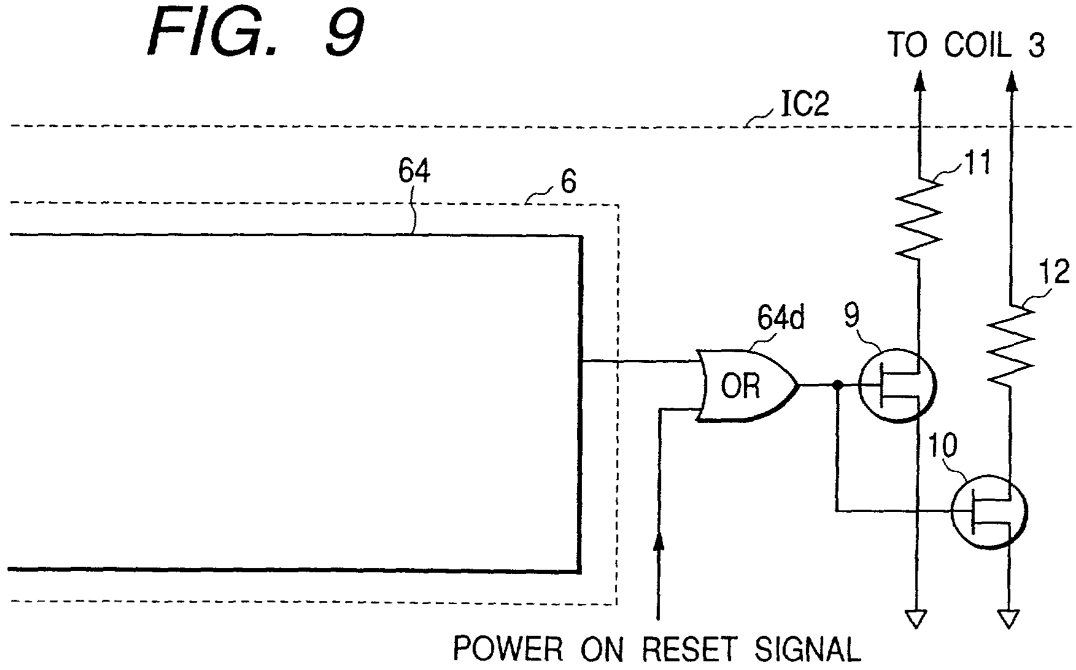

CIRCUIT IS ACTIVE
RELEASE FROM POWER ON RESET
=POWER ON RESET VOLTAGE
=WORKING VOLTAGE
VOLTAGE VARIATION
CAUSED BY RESISTANCE
OUTPUT
VOLTAGE OF
RECTIFIER
TIME

FIG. 9


TO COIL 3
IC2
64
6
11
12
64d
9
OR
10
POWER ON RESET SIGNAL

NTO144US8E

PTO/SB/106(8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

RFID(RADIO FREQUENCY IDENTIFICATION) AND IC CARD

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を__________とし、(該当する場合) __________に訂正されました。

☐ was filed on
as United States Application Number or
PCT International Application Number
__________ and was amended on
__________ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第３７編第１条５６項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration
(日本語宣言書)

私は、米国法典第３５編１１９条 (a) - (d) 項又は３６５条 (b) 項に基き下記の、 米国以外の国の少なくとも一カ国を指定している特許協力条約３６５ (a) 項に基ずく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
2000-067141	Japan	7/ March / 2000	☐
			☐

私は、第３５編米国法典１１９条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第３５編１２０条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約３６５条 (c) に基ずく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第３５編１１２条第１項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第３７編１条５６項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自身の知識に基ずいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基ずく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第１８編第１００１条に基ずき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁護士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (*list name and registration number*)

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（第二以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for second and subsequent joint inventors.)

PTO/SB/106(8-96)
Approved for use through 9/30/98. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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